

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Claims 2, 5, 6, 7, 8, 10, 11, 13, 15, 16, 21, 22, 27, 33, 35 and 37 have been amended.

Listing of Claims:

1. (Previously Presented) An apparatus, comprising:

two or more memories having one or more redundant components associated with each memory, the one or more redundant components include at least one redundant column of memory cells;

a first processor on-chip with the two or more memories and containing redundancy allocation logic to execute one or more repair algorithms to generate a repair signature for each of the two or more memory; and

a repair data container on-chip with the two or more memories and to store a concatenated repair signature, composed by the first processor, that comprises a string of bits arranged as a plurality of fields, one field for each of the memories, (1) for each memory having one or more defective memory cells detected during fault testing, the field consists of (a) a single bit that identifies the memory, followed by (b) a plurality of bits being compressed, repair signature data for the memory, and (2) for each memory with no defective memory cells, the field consists of a single bit that identifies the memory.

2. (Currently Amended) The apparatus of claim 1, wherein the repair data is in

a fuse box located on the same chip but external to area occupied by the two or more memories.

3. (Previously Presented) The apparatus of claim 1, wherein for each memory with no defect the identifier bit directs the processor to bypass loading of reconfiguration data into the memory corresponding to this identifier bit.

4. (Previously Presented) The apparatus of claim 1, wherein for each memory with no defect the identifier bit directs the processor to load a pre-stored series of reconfiguration data bits into scan chain registers of the memory corresponding to this identifier bit but the content of the reconfiguration data bits does not cause a substitution of a redundant component for a non-redundant component in that memory.

5. (Currently Amended) The apparatus of claim 2, wherein the fuse box contains ~~one~~two or more fuses and a fuse is a non-volatile storage device that performs the function of a fuse selected from the group consisting of a Flash memory cell, an Electrically Programmable Read Only Memory cell, a one-time programmable memory cell, a few-time programmable memory cell, and a laser fuse.

6. (Currently Amended) The apparatus of claim 1, wherein the first processor further includes logic internal to the first processor configured to compress an amount of bits making up an actual repair signature for a first memory that has one or more defective memory cells that were actually detected during fault testing of the two or

more memories and logic internal to the first processor configured to determine one or more locations of the one or more defective memory cells detected during fault testing and configured to provide error logging, wherein the actual repair signature is generated for each memory having one or more defective memory cells that were actually detected during fault testing, and the field consists of the single bit that identifies the memory, followed by the plurality of bits being compressed.

7. (Currently Amended) The apparatus of claim 6, wherein the processor further includes logic configured to decompress an amount of bits making up the actual repair signature for the first memory of the two or more memories in the stored concatenated repair signature.

8. (Currently Amended) The apparatus of claim 2, wherein the processor further includes logic configured to compose the concatenated repair signature for all of the memories sharing the fuse box and configured to identify and allocate available redundant rows of memory cells and redundant columns of memory cells in order to determine an optimum redundancy scheme when a failure occurs, wherein the concatenated repair signature is a compilation of repair signatures for the two or more memories, which is stored in the same repair data container and is stored in a format dependent upon whether one or more defective memory cells were detected during fault testing for that particular memory of the two or more memories.

9. (Previously Presented) The apparatus of claim 1, wherein the repair data

container contains an amount of fuses to store (1) actual repair signatures for an adjustable subset of the redundant components associated with the two or more memories and (2) dummy repair signatures for the remaining memories.

10. (Currently Amended) The apparatus of claim 1, wherein the repair data container stores indicator bits for each memory sharing ~~that~~the repair data container, and a presence of an active bit in the indicator bits indicates that the repair data container contains an actual repair signature for that memory having a defect and a dummy repair signature is generated for each memory with no defective memory cells in which the field consists of the single bit that identifies the memory.

11. (Currently Amended) The apparatus of claim 2, wherein the fuse box has a dedicated field for each memory sharing ~~that~~the fuse box, and a presence of an active bit in the dedicated field indicates that the fuse box contains an actual repair signature for that memory having a defect.

12. (Original) The apparatus of claim 1, wherein the processor further includes logic configured to provide built in self-test logic, built-in self-diagnosis logic, and reconfiguration data logic.

13. (Currently Amended) The apparatus of claim ~~4~~6, further comprises:
compression/decompression logic ~~around~~external to the repair data container configured to compress an amount of bits making up ~~at~~the actual repair signature and

decompress an amount of bits making up the actual repair signature.

14. (Canceled).

15. (Currently Amended) The apparatus of claim 1, further comprising:

~~two or more processors including the first processor and a second processor~~
~~wherein the second processor contains~~ing redundancy allocation logic and is coupled to one or more memories discreet from the two or more memories coupled to the first processor, wherein the repair data container is to store the concatenated repair signature that repairs the memories connected to the first processor as well as the memories connected to the second processor.

16. (Currently Amended) An apparatus, comprising:

a repair data container located on a chip, the repair data container to store an actual repair signature for each memory having a defective memory cell;

two or more memories located on the chip, each memory having redundant components that share the repair data container, wherein the repair data container has an amount of fuses to store the actual repair signatures for an adjustable subset of the two or more memories; and

a processor, located on the chip, having logic configured to test the memories during each initialization cycle of operation of the chip and to ~~generate an augmented~~ the actual repair signature if a new defect is detected, the processor to compose a concatenated repair signature that comprises a string of bits arranged as a plurality of

fields one for each memory, for each memory having a defective cell the field consists of one or more bits that identify the memory followed by a plurality of bits being compressed repair signature data for the memory, and for each memory with no defective memory cell the field consists of only one or more bits that identify the memory, wherein the augmented actual repair signature has repair signature data to repair defects detected prior to the operation of the chip as well as defects detected during the initialization cycle of operation of the chip.

17. (Original) The apparatus of claim 16, wherein the repair data container also stores dummy repair signatures for each memory with no defective memory cells.

18. (Previously Presented) The apparatus of claim 17, wherein the processor also contains redundancy allocation logic and is coupled to the repair data container, wherein the repair data container stores a concatenated repair signature that includes the actual repair signatures and the dummy repair signatures.

19. (Previously Presented) The apparatus of claim 17, further comprising:
wherein the processor coupled is to the repair data container, and the processor contains logic configured to decompress an amount of bits making up the actual repair signatures.

20. (Canceled).

21. ((Currently Amended) The apparatus of claim 19, further comprising:

two or more processors at least including the processor as a first processor and a second processor, wherein the second processor containing logic is configured to test and repair a set of memories connected to the second processor discreet from the memories coupled to the first processor; wherein the repair data container has an amount of fuses to store the actual repair signatures for an adjustable subset of the memories connected to the second processor as well as memories connected to the first processor.

22. (Currently Amended) An apparatus, comprising:

a first processor containing logic configured to test and repair two or more memories connected to ~~that~~the first processor;

a second processor containing logic configured to test and repair two or more memories connected to ~~that~~the second processor; and

a fuse box to store a concatenated repair signature that repairs the memories connected to the first processor as well as the memories connected to the second processor, wherein the concatenated repair signature ~~that~~ comprises a string of bits arranged as a plurality of fields one for each memory, for each memory having a defective cell the field consists of one or more bits that identify the memory followed by a plurality of bits being compressed that are the repair signature data for the memory, and for each memory with no defective memory cells the field consists of only one or more bits that identify the memory, and wherein the fuse box contains an amount of non-volatile fuses to provide actual repair capability for only a subset of all of the

memories that share the fuse box.

23. (Original) The apparatus of claim 22, wherein the first processor contains logic configured to decompress an amount of bits making up the concatenated repair signature.

24. (Canceled).

25. (Original) The apparatus of claim 22, wherein the fuse box is located external to the memories.

26. (Previously Presented) The apparatus of claim 22, wherein the processors and the fuse box are embedded on a single chip.

27. (Currently Amended) A method, comprising:

composing a concatenated repair signature for two or more memory cores on every cycle a device containing the two or more memory cores is initialized, wherein the concatenated repair signature comprises a string of bits arranged as a plurality of fields one for each memory core, for each memory core having a defective cell the field consists of one or more bits that identify the memory core followed by a plurality of bits being compressed that are the repair signature data for the memory core, and for each memory core with no defective memory cells the field consists of only one or more bits that identify the memory core;

sending the concatenated repair signature to be stored in non-volatile fuses;
and

decompressing the concatenated repair signature to send reconfiguration data
to the two or more memory cores.

28. (Previously Presented) The method of claim of 27, further comprising:
storing an actual repair signature for a subset of the two or more memory cores
and a dummy repair signature for the remaining memory cores.

29. (Previously Presented) The method of claim of 27, further comprising:
repairing an adjustable subset of memory cores having redundant elements.

30. (Currently Amended) An apparatus, comprising:
means for composing a concatenated repair signature for two or more memory
cores on every cycle a device containing the two or more memory cores is initialized,
wherein the concatenated repair signature comprises a string of bits arranged as a
plurality of fields one for each memory core, for each memory core having a defective
cell the field consists of one or more bits that identify the memory core followed by a
plurality of bits being compressed, which are repair signature data for the memory core,
and for each memory core with no defective memory cells the field consists of only one
or more bits that identify the memory core;

means for sending the concatenated repair signature for each memory core to be
stored in non-volatile fuses; and

means for decompressing the concatenated repair signature to send reconfiguration data to the two or more memory cores.

31. (Previously Presented) The apparatus of claim of 30, further comprising:

means for storing an actual repair signature for a subset of the two or more memory cores and a dummy repair signature for the remaining memory cores.

32. (Previously Presented) The apparatus of claim of 30, further comprising:

means for repairing an adjustable subset of memory cores having redundant elements.

33. (Currently Amended) A machine readable medium that stores data and executable instructions representing an integrated circuit, which when executed by a machine to cause the machine to generate a representation of the integrated circuit including:

a first processor containing logic configured to test and repair two or more memories connected to that first processor;

a second processor containing logic configured to test and repair two or more memories connected to that second processor; and

a fuse box to store a concatenated repair signature that repairs the memories connected the first processor as well as the memories connected to the second processor, wherein the fuse box contains an amount of non-volatile fuses to provide actual repair capability for only a subset of all of the memories that share

the fuse box.

34. (Previously Presented) The machine-readable medium of claim 33, wherein the machine-readable medium comprises a memory compiler to provide a layout utilized to generate one or more lithographic masks used in the fabrication of the fuse box and the processors.

35. (Currently Amended) A machine readable medium that stores data and executable instructions representing an integrated circuit, which when executed by a machine to cause the machine to generate a representation of the integrated circuit including:

a repair data container located on a chip, the repair data container to store concatenated repair signature ; and

two or more memory cores having redundant components that share the repair data container, wherein the repair data container has an amount of fuses to store the concatenated repair signature for an adjustable subset of the two or more memory cores; and

a processor having logic configured to test the memory cores during each initialization cycle of their operation and to ~~generate an augmented concatenated~~ an actual repair signature if a new defect is detected, wherein the concatenated repair signature comprises a string of bits arranged as a plurality of fields one for each memory core, for each memory core having a defective cell the field consists of one or more bits that identify the memory core followed by a plurality of bits being compressed,

which are repair signature data for the memory core, and for each memory core with no defective memory cells the field consists of only one or more bits that identify the memory core.

36. (Previously Presented) The machine-readable medium of claim 35, wherein the machine-readable medium comprises a memory compiler to provide a layout utilized to generate one or more lithographic masks used in the fabrication of the repair data container and the two or more memory cores.

37. (Previously Presented) A machine readable medium that stores data and executable instructions representing an integrated circuit, which when executed by a machine to cause the machine to generate a representation of the integrated circuit including:

two or more memories having one or more redundant components associated with each memory, the one or more redundant components include at least one redundant column of memory cells;

a processor containing redundancy allocation logic to execute one or more repair algorithms to generate a concatenated repair signature for repair of all of the memories coupled to the processor; and

a repair data container to store the concatenated repair signature, wherein the concatenated repair signature comprises a string of bits arranged as a plurality of fields one for each memory, for each memory having a defective cell the field consists of one or more bits that identify the memory followed by a plurality of bits being

compressed, which are repair signature data for the memory, and for each memory with no defective memory cells the field consists of only one or more bits that identify the memory, wherein the repair data container contains an amount of non-volatile fuses to provide actual repair capability for only a subset of all of the memories that share the fuse box.

38. (Previously Presented) The machine-readable medium of claim 37, wherein the machine-readable medium comprises a memory compiler to provide a layout utilized to generate one or more lithographic masks used in the fabrication of the repair data container, the processor, and the two or more memories.